Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action. Claims 1-47 are presented herewith for consideration.

Claims 4 and 9 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

Claims 1, 3, 6, 8 and 25-47 are rejected under 35 U.S.C. §102(a) as being anticipated by previously cited the alleged "Admitted Prior Art" (APA).

Claims 11-12 and 13-14 are rejected under 35 U.S.C. §102(a) as being anticipated by newly cited U.S. Patent No. 6,392,457 B1 (*Ransijn*).

Claims 2, 7 and 21-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of previously cited U.S. Patent No. 5,859,550 (*Brandt*).

Claims 4-5, 9-10 and 15-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of *Ransijn*.

I. Rejection of Claims 4 and 9 under 35 U.S.C. §112

Claims 4 and 9 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

The applicant's attorney respectfully disagrees. Illustration and description of embodiments of claims 4 and 9 may, at the very least, be seen in Fig. 5 and at pages 11 and 12. Please also note at page 11, line 15 of the instant Specification: "Fig. 5 illustrates yet another application of the phase detection using the concepts already discussed [Figs. 3 and 4]." Accordingly, embodiments of claims 4 and 9 may include a combination of the described phase detection and plurality of clock generation and calibration circuits shown in Fig. 5.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 4 and 9 under 35 U.S.C. §112, first paragraph.

II. Rejection of Claims 1, 3, 6, 8 and 25-47 under 35 U.S.C. §102(a)

Claims 1, 3, 6, 8 and 25-47 are rejected under 35 U.S.C. §102(a) as being anticipated by APA.

In rejecting claim 1, the Examiner stated:

> APA Fig. 2 discloses a device comprising: a first clock generator (20 & 22) receiving a first digital value (PHASE1) to generate a first clock signal (CLK1); a second clock generator (20 & 23) receiving a second digital control value (PHASE2) to generate a second clock signal (CLK2); and a phase detection logic (31) comparing CLK1 and

CLK2 to detect a phase relationship between the first and second clock signals…Office Action, page 5. (Emphasis added.)

However, in direct contrast, claim 1 calls for "comparing the first and second digital control values" and **not** comparing the first and second clock signals-- "CLK1" and "CLK2" as stated by the Examiner. (Emphasis added.) As clearly illustrated in Fig. 2, PHASE1 and PHASE2 are not even input to phase detection circuit 31, but rather respectively input to phase shifters 22 and 23. Accordingly, phase detection circuit 31 can not "compare the first and second digital control values to detect a phase relationship between the first and second clock signals."

Independent claim 6 includes similar limitations and therefore is patentable for at least the reasons stated above in regard to claim 1.

Claims 3 and 8 depend from claims 1 and 6 and therefore are patentable for at least the reasons stated above in regard to independent claims 1 and 6.

In rejecting claims 25, 34 and 41, the Examiner stated:

> [I]n Fig. 2, the APA discloses a device and its method, the device comprises: an input clock generator (a clock generator generating the input timing signal CLK1) with the setting PHASE1 value related to a target timing signal (CLK2) generated with reference source element 20 by setting a phase control value (PHASE2)…an evaluation logic (the phase detection circuit 31) to evaluate and compare the phase values of the two clock signals CLK1 and CLK2…Office action, page 6. (Emphasis added.)

As described above and clearly shown in Fig. 2, PHASE1 and PHASE2 are not input into phase detection circuit 31 so phase detection circuit 31 can not "evaluate and compare the phase values of the two clock signals CLK1 and CLK2" as stated by the Examiner.

Further, claim 25 calls for "setting the input phase control value to calibrate the phase of the input timing signal relative to the received data signal." In rejecting claim 25, the Examiner stated that "the input timing signal" corresponds to "CLK1" but contradictorily stated that the "phase control value" corresponds to "PHASE2." However, Fig. 2 clearly illustrates that a PHASE2 value adjusts clock signal CLK2 and not CLK1 or the "input timing signal" as stated by the Examiner.

Independent claims 34 and 41 include similar limitations and therefore are patentable for at least the reasons stated above in regard to claim 25.

Dependent claims 26-33, 35-40 and 42-47 depend from independent claims 25, 34 and 41 and therefore are patentable for at least the reasons stated above in regard to independent claims 25, 34 and 41.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 1, 3, 6, 8 and 25-47 under 35 U.S.C. §102(a).

III. Rejection of Claims 11-12 and 13-14 under 35 U.S.C. §102(a)

Claims 11-12 and 13-14 are rejected under 35 U.S.C. §102(a) as being anticipated by *Ransijn*.

In rejecting claims 11-12 and 13-14, the Examiner has contradictorily stated that the "CLK2/CLOCK" signal as disclosed by *Ransijn* corresponds to both the claimed "reference clock signal" and the "phase control value." Office Action, page 7. The Examiner appears to lump the two different signals together when claim 11 clearly calls for a "reference clock signal" and a "phase control value."

Further, the Examiner has stated that the claimed "measurement clock signal" corresponds to the "CLK1" signal as disclosed by *Ransijn*. However, Fig. 5 of *Ransijn* shows that the "CLK1" signal appears to be the same as the "CLOCK" signal—both output from "VCO 16." Thus, the Examiner has not clearly stated which signal as disclosed by *Ransijn* corresponds to which particular claimed element without using the same signal for distinctly different claim elements.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims11-12 and 13-14 under 35 U.S.C. §102(a).

IV. Rejection of Claims 2, 7 and 21-24 under 35 U.S.C. §103(a)

Claims 2, 7 and 21-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of *Brandt*.

Claims 2 and 7 depend from independent claims 1 and 6 and therefore are patentable for at least the reasons stated above in regard to independent claims 1 and 6.

In rejecting claim 21, the Examiner stated that:

> [I]t would have been obvious to a [sic] one of ordinary skill in the art at the time the invention was make [sic, made] to have the PVT-compensated circuit as taught by Brandt in the device of APA that the PVT-compensated circuit takes the output of the Phase detection circuit 31 receiving CLK1 and CLK2 as inputs to compensate the process, voltage, and temperature variations for the purpose to reduce the clock skew and get accurate clock signals…Office Action, page 8.

Claims 21 and 23 call for "varying the phase control value to obtain a digital PVT adjustment value that provides a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal…" and claim 23 calls for "a calibration logic to vary the phase control value to obtain a digital PVT adjustment value…"(Emphasis added.)

The Examiner has not identified where the APA and/or *Brandt* disclose or suggest such a limitation. Further as stated above, PHASE1 and PHASE2 are not input to phase detection circuit 31 of the APA, so phase detection circuit 31 can not "vary[ing] the phase control value [PHASE1 or PHASE2] to obtain a digital PVT adjustment value…" as suggested by the Examiner.

Claims 22 and 24 depend from independent claims 21 and 23 and therefore are patentable for at least the reasons stated above in regard to independent claims 21 and 23.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 2, 7 and 21-24 under 35 U.S.C. §103(a).

V. Rejection of Claims 4-5, 9-10 and 15-20 under 35 U.S.C. §103(a)

Claims 4-5, 9-10 and 15-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of *Ransijn*.

In rejecting claims 4 and 9, the Examiner stated:

> APA does not explicitly specify the calibration logic to set the second digital control value CLK2 (or CLK1 depending which one is the first and the second). Office Action, page 10. (Emphasis added.)

Once again, the Examiner has contradictory reasons in rejecting claims 4 and 9 as compared to the stated rejection of claim 1 above. In rejecting claim 1, the Examiner stated that signals CLK1 and CLK2 of APA are "clock signals," but in rejecting claims 4 and 9 the Examiner has stated CLK1 and CLK2 of APA are "digital control value[s]."

Claims 5 and 10 are patentable for at least the reasons stated above in regard to claims 4 and 9.

In rejecting claim 15, the Examiner stated the APA discloses "a calibration logic (the phase detection 31) deriving correction values (on 30) producing the phase differences/relationships…"Office Action, page 12.

Claim 15 calls for "deriving a plurality of correction values from the digital control values that provide the predetermined phase relationships…" As stated above, Fig. 5 of APA does not receive the "digital control values" (PHASE1 and PHASE2) so that phase detection 31 can not "derive a plurality of correction values from the digital control values…"

Claims 16-17 depend from claim 15 and therefore are patentable for at least the reasons stated above in regard to independent claim 15.

Claim 18 is patentable for at least similar reasons stated above in regard to claim 15.

Claims 19-20 depend from claim 18 and therefore are patentable for at least the reasons stated above in regard to independent claim 18.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 4-5, 9-10 and 15-20 under 35 U.S.C. §103(a).

VI. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-47 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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